NON-VOLATILE MEMORY CELLS HAVING FLOATING GATE AND METHOD OF FORMING THE SAME

ABSTRACT OF THE DISCLOSURE

A non-volatile memory cell having a floating gate and a method of forming the same. The non-volatile memory cell includes a device isolation layer that is formed in a semiconductor substrate and defines an active region. A floating gate is disposed over the active region and is comprised of a plurality of first conductive patterns and a plurality of second conductive patterns that are alternately stacked. A first insulation layer is disposed between the floating gate and the active region. One of the first conductive pattern and the second conductive pattern protrudes to form concave and convex sidewalls of the floating gate. Therefore, a surface area of the floating gate increases, thereby raising coupling ratio between the floating gate and the control gate electrode. As a result, an operating voltage of the non-volatile memory cell can be reduced.